Electronic Version
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Claims

[c1] 1. A DRAM cell, comprising:
a deep trench capacitor; and
a transistor, comprising
a semiconductor pillar beside the deep trench capacitor not overlapping with the deep-trench capacitor;
a multi-gate at least on three sidewalls of the pillar;
a gate dielectric layer between the pillar and the multi-gate;
a first source/drain region in a top portion of the pillar; and
a second source/drain region in a lower portion of the pillar apart from the first source/ drain region, coupling with the deep trench capacitor.

[c2] 2. The DRAM cell of claim 1, wherein the multi-gate is a treble gate on three sidewalls of the pillar, the three sidewalls including a first sidewall facing the deep trench capacitor and a second and a third sidewalls adjacent to the first sidewall.

[c3] 3. The DRAM cell of claim 2, wherein a top surface of the treble gate is lower than a top surface of the pillar.

[c4] 4. The DRAM cell of claim 3, wherein the first source/drain region takes the whole area of the top portion of the pillar.

[c5] 5. The DRAM cell of claim 2, wherein the treble gate further covers a portion of a top surface of the pillar.

[c6] 6. The DRAM cell of claim 5, wherein the treble gate comprises:
a doped polysilicon layer on the three sidewalls and the top of the pillar; and
a metal comprising layer on the doped polysilicon layer.

[c7] 7. The DRAM cell of claim 5, further comprising a capping layer on the treble gate and a spacer on sidewalls of the treble gate.

[c8] 8. The DRAM cell of claim 1, wherein the multi-gate is a surrounding gate that surrounds sidewalls of the pillar.

[c9] 9. The DRAM cell of claim 8, wherein the width of the pillar is smaller than a feature size.

[c10] 10. The DRAM cell of claim 9, wherein the width of the pillar is sufficiently small for inducing full depletion therein in use of the DRAM cell.

[c11] 11. The DRAM cell of claim 8, wherein a top surface of the surrounding gate is lower than a top surface of the

pillar.

[c12] 12. The DRAM cell of claim 11, wherein the first source/ drain region takes the whole area of the top portion of the pillar.

[c13] 13. The DRAM cell of claim 1, wherein the second source/drain region is also a buried strap electrically connecting with an inner electrode of the deep trench capacitor.

[c14] 14. A DRAM array, comprising:
a plurality of deep trench capacitors, arranged in rows and columns;
a plurality of transistors, each being disposed adjacent to at least one deep trench capacitor along the column direction and comprising:
a semiconductor pillar beside the deep trench capacitor not overlapping with the deep-trench capacitor;
a multi-gate at least on three sidewalls of the pillar;
a gate dielectric layer between the pillar and the multi-gate;
a first source/drain region in a top portion of the pillar; and
a second source/drain region in a lower portion of the pillar apart from the first source/ drain region, coupling with the deep trench capacitor;

a plurality of word lines, each being coupled with the multi-gates of the transistors in one row; and
a plurality of bit lines, each being coupled with the first source/drain regions of the transistors in one column.

[c15] 15. The DRAM array of claim 14, wherein the second source/drain region of each transistor is also a buried strap electrically connecting with an inner electrode of the corresponding deep trench capacitor.

[c16] 16. The DRAM array of claim 14, wherein each multi-gate is a treble gate on three sidewalls of the corresponding pillar.

[c17] 17. The DRAM array of claim 16, wherein a pair of adjacent transistors in a column share a pillar and a first source/drain region, and two deep trench capacitors corresponding to the pair of adjacent transistors are disposed at two opposite sides of the shared pillar along the column direction.

[c18] 18. The DRAM array of claim 17, which is a sub-$6F^2$ memory array.

[c19] 19. The DRAM array of claim 16, wherein a top surface of each treble gate is lower than a top surface of the corresponding pillar.

[c20] 20. The DRAM array of claim 19, wherein each first source/drain region takes the whole area of the top portion of the corresponding pillar.

[c21] 21. The DRAM array of claim 19, wherein the bit lines directly contact with the first source/drain regions in one column.

[c22] 22. The DRAM array of claim 16, wherein each treble gate further covers a portion of a top surface of the corresponding pillar.

[c23] 23. The DRAM array of claim 22, wherein each treble gate comprises:
a doped polysilicon layer on three sidewalls and the top of the pillar; and
a metal comprising layer on the doped polysilicon layer.

[c24] 24. The DRAM array of claim 22, wherein each treble gate is further disposed with a capping layer thereon and a spacer on sidewalls thereof.

[c25] 25. The DRAM array of claim 24, wherein the bit lines electrically connect with the first source/drain regions via self-aligned contacts (SAC).

[c26] 26. The DRAM array of claim 14, wherein each multi-gate is a surrounding gate that surrounds sidewalls of

the corresponding pillar.

[c27] 27. The DRAM array of claim 26, wherein the width of the pillar is smaller than a feature size.

[c28] 28. The DRAM array of claim 27, wherein the width of the pillar is sufficiently small for inducing full depletion therein in use of the DRAM array.

[c29] 29. The DRAM array of claim 26, wherein each transistor is disposed on the same side of the corresponding deep trench capacitor along the column direction.

[c30] 30. The DRAM array of claim 29, which is a $4F^2$ memory array.

[c31] 31. The DRAM array of claim 26, wherein a top surface of each surrounding gate is lower than a top surface of the corresponding pillar.

[c32] 32. The DRAM array of claim 31, wherein each first source/drain region takes the whole area of the top portion of the corresponding pillar.

[c33] 33. The DRAM array of claim 31, wherein the bit lines directly contact with the first source/drain regions.

[c34] 34. A DRAM process, comprising:
forming a deep trench capacitor in a semiconductor sub-

strate;

defining an active area over the substrate to form a semiconductor pillar beside the deep trench capacitor and to form an isolation area;

forming a buried strap coupling with the deep trench capacitor in the substrate;

forming a gate dielectric layer on the pillar;

forming a word line including a multi-gate over the substrate, wherein the multi-gate is at least on three sidewalls of the pillar and is separated from the pillar by the gate dielectric layer;

forming a source/drain region in a top portion of the pillar; and

forming a bit line electrically connecting with the source/drain region,

wherein the pillar, the buried strap, the gate dielectric layer, the multi-gate and the source/drain region together constitute a transistor.

[c35] 35. The DRAM process of claim 34, wherein the buried strap is formed through out-diffusion of dopants from a contact portion of an inner electrode of the deep trench capacitor.

[c36] 36. The DRAM process of claim 34, wherein a mask layer for defining the active area overlaps with the deep trench capacitor.

[c37] 37. The DRAM process of claim 34, wherein the multi-gate is formed as a treble gate on three sidewalls of the pillar.

[c38] 38. The DRAM process of claim 37, wherein forming the gate dielectric layer and the word line including the treble gate comprises:
filling the isolation area with an insulating material;
recessing the insulating material to expose a first, a second, and a third sidewalls of the pillar above a predetermined level, wherein the first sidewall faces the deep trench capacitor and the second and third sidewalls are adjacent to the first sidewall;
forming a gate dielectric layer on the pillar;
forming a conductive layer over the substrate; and
patterning the conductive layer to form a word line including a treble gate, wherein the treble gate is formed on the first to third sidewalls and the top of the pillar.

[c39] 39. The DRAM process of claim 38, wherein the step of forming the source/drain region in the top portion of the pillar comprises:
performing an ion implantation process using the word line as a mask.

[c40] 40. The DRAM process of claim 38, wherein the conduc-

tive layer comprises a doped polysilicon layer and a metal comprising layer on the doped polysilicon layer.

[c41] 41. The DRAM process of claim 38, further comprising:
forming a capping layer on the conductive layer before the conductive layer is patterned, while the capping layer and the conductive layer are patterned successively to form a stacked word line structure; and
forming a spacer on sidewalls of the stacked word line structure.

[c42] 42. The DRAM process of claim 41, further comprising a step of forming a self-aligned contact (SAC) on the source/drain region before the bit line is formed for electrically connecting the source/drain region and the bit line.

[c43] 43. The DRAM process of claim 37, wherein forming the gate dielectric layer and the word line including the treble gate comprises:
filling the isolation area with an insulating material;
patterning the insulating material to form a trench in which the word line will be formed, the trench exposing a first sidewall of the pillar above a predetermined level and a portion of a second sidewall and a portion of a third sidewall of the pillar above the predetermined level, wherein the first sidewall faces the deep trench capacitor

and the second and third sidewalls are adjacent to the first sidewall;
forming a gate dielectric layer on the pillar; and
forming the word line in the trench.

[c44] 44. The DRAM process of claim 43, wherein a top surface of the word line is lower than a top surface of the pillar.

[c45] 45. The DRAM process of claim 44, wherein the step of forming the bit line comprises:
forming an insulating layer in the trench covering the word line; and
forming a patterned conductive layer as a bit line directly contacting with the source/drain region.

[c46] 46. The DRAM process of claim 34, wherein the multi-gate is formed as a surrounding gate that surrounds sidewalls of the pillar.

[c47] 47. The DRAM process of claim 46, wherein the width of the pillar is smaller than a feature size.

[c48] 48. The DRAM process of claim 47, wherein the width of the pillar is sufficiently small for inducing full depletion therein in use of the DRAM cell.

[c49] 49. The DRAM process of claim 46, wherein forming the gate dielectric layer and the word line including the sur-

rounding gate comprises:

filling the isolation area with an insulating material;

patterning the insulating material to form a trench in which the word line will be formed, the trench exposing all sidewalls of the pillar above a predetermined level;

forming a gate dielectric layer on the pillar; and

forming the word line in the trench.

[c50] 50. The DRAM process of claim 49, wherein a top surface of the word line is lower than a top surface of the pillar.

[c51] 51. The DRAM process of claim 50, wherein the step of forming the bit line comprises:

forming an insulating layer in the trench covering the word line; and

forming a patterned conductive layer as a bit line directly contacting with the source/drain region.